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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,668	12/31/2003	Chao-Cheng Lee	TOP 347	2785
23995	7590	02/02/2005	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			LE, DINH THANH	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 02/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/748,668

Applicant(s)

LEE ET AL.

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7 are rejected under 35 USC 103 (a) as being unpatentable over Lennous et al (US 6,608,516) in view of Yamakido et al (US 4,250,492).

Lennous et al discloses in Figure 1 a filter circuit comprising:

- a transconductance device (OA1) for outputting a current signal according to an input voltage (IN) and a feedback voltage;
- a transresistance device (16A) coupled to the transconductance device (OA1) for outputting a output voltage according to the current signal;
- wherein the transresistance device (16A) comprises: a first capacitor (C1); a resistor (R6) coupled to the capacitor (C1) and the transconductance device (OA3)

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- wherein a time constant of the filter circuit is determined by the first capacitor (C1) and the resistor (R6); and a feedback device coupled between the transconductance device (OA1) and the transresistance device (OA3) for outputting the feedback voltage according to the output voltage. wherein the transconductance device (OA1) comprises: a first operational amplifier having a first non-converting input coupled to a ground, a first converting input terminal and a first output terminal to output the current signal;
- wherein the transresistance device (16A) comprises: a second operational amplifier (OA3) having a second non-converting input terminal coupled to a ground, a second converting input terminal and a second output terminal to output the output voltage; the first capacitor (C1) coupled to the second output terminal and the second converting input terminal; and the resistor (R6) coupled to the second converting input terminal for receiving the current signal; and
- wherein the feedback device comprises: a third operational amplifier (OA2) having a third non-converting input terminal coupled to a ground, a third converting input terminal and a third output terminal to output the output voltage; a third resistor (R5) coupled to the third output terminal and the third converting input terminal; and a fourth resistor (R3) coupled to the third output terminal for outputting the feedback voltage.

However, Lennous et al does not disclose that the resistor (R6) is an attenuator comprising a plurality of stages connected serially, wherein each stage of the resistor network comprises: an input node; an output node; a first resistor coupled between the input node and the ground; and a second resistor coupled between the input node and the output node.

Yamakido et al teaches in Figure 3 a resistive network comprising a plurality of resistors

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stages each including a first resistor (2R) and a second (R) for providing a selectable attenuations to attenuate the magnitude of the input signal. It would have been obvious to a person having skill in the art at the time the invention was made to employ the selectable attenuator taught by Yamakido et al in the circuit of Lennous et al for the purpose of providing selectable attenuations to attenuate the magnitude of the input signal.

With regard to claim 6, although Yamakido et al does not disclose that each of the first resistor and the second resistor is implemented by a MOS transistor; however, the MOS transistor is configured to perform the function of a resistor for easily fabricated on an integrated circuit is well known the art. It would have been obvious to a person having skill in the art to employ the MOS transistor in the modified circuit of Lennous et al for the purpose easily implementing on an IC chip so that the size and the weight of the modified circuit would be reduced.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Dinh Le', with a long horizontal flourish extending to the right.

DINH LE

Primary Examiner